# **23EC2103–DIGITAL CIRCUITS DESIGN**

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| **CourseCategory:** | Professional Core | **Credits:** | 3 |
| **CourseType:** | Theory | **Lecture-Tutorial-****Practical:** | 3-0-0 |
| **Prerequisite:** | Number systems,Boolean Algebra. | **Sessional Evaluation:Univ.ExamEvaluation:****TotalMarks:** | 3070100 |
| **CourseObjectives** | * Understand the properties of Boolean algebra ,logic operations ,and minimization of Boolean functions.
* Analyze combinational and analyze sequential logic circuits.
* Understand the concepts of FSM and compare various Programmable logic devices.
* Model combinational and sequential circuits using HDLs.
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| **CourseOutcomes** | Upon successful completion of the course, the students will be able to: |
| CO1 | Understand the properties of Boolean algebra ,logic operations ,concepts of FSM( L2) |
| CO2 | Apply techniques for minimization of Boolean functions(L3) |
| CO3 | Analyze combinational and Sequential logic circuits.(L4) |
| CO4 | Compare various Programmable logic devices.(L4) |
| CO5 | Design and Model combinational and sequential circuits using HDLs.(L5,L6) |
| **CourseContent** | **UNIT-I**Boolean algebra, logic operations, and minimization of Boolean functions, Review of Number Systems and Codes ,Representation of unsigned and signed integers, Floating Point representation of real numbers, Laws of Boolean Algebra, Theorems of Boolean Algebra, Realization of functions using logic gates ,Canonical forms of Boolean Functions ,Minimization of Functions using Karnaugh Maps.**UNIT-II****Combinational Logic Circuits:** Combinational circuits, Design with basic logic gates, design procedure, adders, subtractors, 4-bit binary adder/ subtractor circuit, BCD adder,carrylook-a-head adder ,binary multiplier ,magnitude comparator, data selectors, priority encoders,decoders,multiplexers, demultiplexers.**UNIT-III****Hardware Description Language:** Introduction to Verilog - structural specification of logic circuits, behavioral specification of logic circuits ,hierarchical Verilog Code, Verilog for combinational circuits-conditional operator ,if-else statement, case statement ,for loop usings equential circuits with CAD tools.**UNIT-IV****Sequential Logic Circuits:** Basic architectural distinction between combinational and sequential circuits ,Design procedure ,latches ,flip-flops ,truth tables and excitation tables, timing and triggering consideration, conversion of flip- flops, design of counters ,ripple counters, synchronous counters, ringcounter, Johnson counter, registers,shift |

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|  | Registers ,universal shift register .Verilog constructs fors equential circuits, flip-flop with clear capability, using Verilog constructs for registers and counters.**UNIT-V****Finite State Machines and Programmable Logic Devices:** Types of FSM, capabilities and limitations of FSM, state assignment, realization of FSM using flip-flops, Mealy to Moore conversion and vice-versa, reduction of state tables using partition technique ,Design of sequence detector. Types of PLD’s: PROM, PAL, PLA, basic structure of CPLD and FPGA,advantages of FPGAs. |
|  | **TEXTBOOKS:** |
|  | 1. M.MorrisMano,“DigitalDesign”,3rdEdition,PHI.(UnitItoIV)
2. StephenBrownandZvonkoVranesic,“FundamentalsofDigitalLogicwithVerilogDesign”,3rdEdition,McGraw-Hill(UnitV)
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| **Text Books&ReferenceBooks** | **REFERENCEBOOKS:**1. CharlesH.Roth,Jr,“FundamentalsofLogicDesign”,4thEdition,JaicoPublishers.
2. ZviKohaviandNirajK.Jha,“SwitchingandFiniteAutomataTheory,3rdEdition,CambridgeUniversityPress,2010.
3. SamirPalnitkar,“VerilogHDL:AGuidetoDigitalDesignandSynthesis”,2ndEdition,Prentice HallPTR.
4. D.P.Leach,A.P.Malvino,“DigitalPrinciplesandApplications”,TMH,7thEdition.
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| Contribution of Course Outcomes towards achievement of Program Outcomes (3-High, 2-Medium, 1-Low) |
|  | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
| CO1 | 3 | 3 | 2 | 2 | - | - | - | - | - | - | - | - | 3 | 2 |
| CO2 | 3 | 3 | 2 | 2 | - | - | - | - | - | - | - | - | 3 | 2 |
| CO3 | 3 | 3 | 2 | 2 | - | - | - | - | - | - | - | - | 3 | 2 |
| CO4 | 3 | 3 | 2 | 2 | - | - | - | - | - | - | - | - | 3 | 2 |
| CO5 | 3 | 3 | 2 | 2 | 3 | - | - | - | - | - | - | - | 3 | 2 |